

**IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE**

Patent Application

Inventors(s): John Michael Hergenrother
Pranav Kalavade

Case: 10-2

Serial No.:

Filing Date:

Examiner: H. Jey Tsai (in the parent)

Group Art Unit: 2812 (in the parent)

Title: Ultra Thin Body Vertical Replacement Gate MOSFET

**THE COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, DC 20231**

SIR:

INFORMATION DISCLOSURE STATEMENT

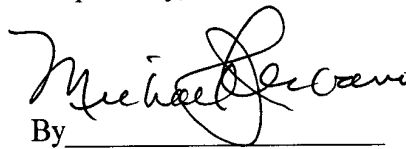
In accordance with 37 CFR 1.98(d), the enclosed Information Disclosure Statement (IDS) of the parent application SN 10/164,202 filed on June 6, 2002 is submitted for consideration in the above-identified application.

No copies of the reference(s) listed in the IDS are enclosed.

NO FEE IS REQUIRED.

In the event of any non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit Agere Systems Inc. Deposit Account No. 501735 as required to correct the error.

Respectfully,



By _____

Michael J. Urbano
Attorney for Applicant(s)
Reg. No. 24522
610-691-7710

Date: 08/26/03

Att. IDS w/o reference(s)

FORM PTO-1449 (REV. 1-84)	U.S. DEPARTMENT OF COMMERCE PATENT & TRADEMARK OFFICE	CASE NO. 7-1	SERIAL NO: 10/164,202
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT: J. M. Hergenrother et al.	
		FILING DATE: June 6, 2002	GROUP: 2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE IF APPROPRIATE						
	AA	6	1	9	7	6	4	1	3/01	Hergenrother et al.	438	268	
	AB												
	AC												
	AD												
	AE												
	AF												
	AG												
	AH												
	AI												
	AJ												
	AK												

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY/AUTHOR	CLASS	SUB- CLASS	TRANSL'N YES NO
	AL						
	AM						
	AN						
	AO						
	AP						

OTHER (Including Author, Title, Date, Pertinent Pages, Etc.)

AR	Ishiwara et al., <i>Lateral solid phase epitaxy in selectively P-doped amorphous Si films</i> , Appl. Phys. Lett., Vol. 49, No. 20, p. 1365 (Nov. 1986) (Abstract only)
AS	Ishiwara et al., <i>Selective Surface Doping Method of P Atoms in Lateral Solid Phase Epitaxy...</i> , Jpn. J. Appl. Phys., Vol. 31, p. 1695 (June 1992)
AT	Dan et al., <i>Lateral solid phase epitaxy of amorphous Si films by selective surface doping method of P atoms</i> , Appl. Phys. Lett., Vol. 53, No. 26, p. 2626 (Dec. 1988)
AU	Greene et al., <i>Thin Single Crystal Silicon on Oxide by Lateral Solid Phase Epitaxy of Amorphous Silicon and Silicon Germanium</i> , Mat. Res. Soc. Symp. Proc., Vol. 609, p. A9.31 (2000)
AV	Choi et al., <i>Ultra-thin-Body SOI MOSFET for Deep-sub-tenth Micron Era</i> , IEEE Electron Dev. Lett., Vol. 21, No. 5, p. 254 (May 2000)
AW	Subramanian et al, <i>A Bulk-Si-compatible Ultrathin SOI Technology for sub-100nm MOSFETs</i> , Device Research Conf. Tech. Dig., p. 28 (1999)
AX	Hergenrother et al, <i>The Vertical Replacement-Gate...Gate Length</i> , IEDM Tech. Dig., p. 75 (1999)
AY	Oh et al, <i>50 nm Vertical Replacement-Gate (VRG) pMOSFETs</i> , IEDM Tech. Dig., p. 65 (2000)
AZ	Hergenrother et al, <i>50 nm Vertical Replacement-Gate (VRG) nMOSFETs with ALD ...Dielectrics</i> , IEDM Tech. Dig., p. 51 (2001)
BA	Hergenrother et al, <i>The Vertical Replacement-Gate MOSFET</i> , Proc. 2 nd European Workshop on the Ultimate Integration of Silicon (ULIS), p. 1 (2001)

EXAMINER:
SHEET 1 OF 1

DATE CONSIDERED: